



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/620,649	07/20/2000	Cetin Nmi Kaya	TI-23686.I	4313

7590 04/06/2005

Jacqueline J Garner Esq  
Texas Instruments Incorporated  
P O Box 655474 M S 219  
Dallas, TX 75265

EXAMINER
----------

WILCZEWSKI, MARY A

ART UNIT	PAPER NUMBER
----------	--------------

2822

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.



UNITED STATES PATENT AND TRADEMARK OFFICE

---

Commissioner for Patents  
United States Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

**MAILED**

APR 06 2005

**GROUP 2800**

Application Number: 09/620,649  
Filing Date: July 20, 2000  
Appellant(s): KAYA, CETIN NMI

---

Jay M. Cantor  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed July 14, 2004.

**(1) *Real Party in Interest***

A statement identifying the real party in interest is contained in the brief.

**(2) *Related Appeals and Interferences***

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

**(3) *Status of Claims***

The statement of the status of the claims contained in the brief is correct.

**(4) *Status of Amendments After Final***

No amendment after final has been filed.

**(5) *Summary of Invention***

The summary of invention contained in the brief is correct.

**(6) *Issues***

The appellant's statement of the issues in the brief is correct.

**(7) Grouping of Claims**

The claims stand or fall together.

**(8) Claims Appealed**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(9) Prior Art of Record**

The following is a listing of the prior art of record relied upon in the rejection of the claims under appeal.

6,051,467	Chan et al.	4-2000
6,001,689	Van Buskirk et al.	12-1999
5,926,711	Woo et al.	7-1999

**(10) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

Art Unit: 2822

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 12, 13, 15, and 16 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Van Buskirk, U.S. Patent 6,001,689, of record.

Van Buskirk et al. disclose an integrated circuit comprising a floating gate memory array wherein the array comprises a plurality of gate stacks having a channel dielectric (61, 62, 63), a polysilicon floating gate (51, 52, 53), a dielectric region disposed outwardly from the floating gate (71, 72, 73), and a polysilicon gate electrode (41, 42, 43), and a plurality of dielectric isolation regions disposed between the gate stacks (26, 27, 28, and 29), see Fig. 2A and column 4, lines 1-10. The structure further comprises trenches and moats (Fig. 7A) formed between the stacks (column 5, lines 35-55). First oxide spacers (120-125) and oxide layer (101) are formed between the gate stacks and subsequently planarized to expose the polysilicon gate (41, 42, 43)(column 5, lines 35-65).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk et al. (U.S. Patent 6,001,689) in view of Woo et al. (U. S. Patent 5,926,711).

Van Buskirk et al. is applied as above. Van Buskirk et al. lacks anticipation only of using hemispherical grains of silicon as the floating gate. Woo et al. teach a floating gate transistor wherein the floating gate (24C) is formed of hemispherical grains of silicon (Fig. 3F and column 4, lines 35-55). It would have been obvious to one of ordinary skill in the art to use a floating gate having hemispherical grains of silicon in order to improve the capacitive coupling of the floating and control gates.

Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk et al. (U.S. Patent 6,001,689) in view of Chen et al. (U. S. Patent 6,051,467).

Van Buskirk et al. is applied as above. Van Buskirk et al. lacks anticipation only of the thickness of the oxide layer in the ONO integrate dielectric. Chan et al. teach that a typical thickness for the oxide layer in an ONO integrate dielectric is between 50 and 100 angstroms (column 3, lines 40-50). It would have been obvious to one skilled in the art to use an oxide layer having a thickness of 50 to 100 angstroms in the known method of Van Buskirk et al. because it is well known to do so, as evidenced by Chan et al., and because this oxide layer thickness provides sufficient gate separation and capacitive coupling. Further, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose particular thicknesses because Applicant

Art Unit: 2822

has not disclosed that the claimed thicknesses are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using thicknesses other than those claimed. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

**(11) Response to Argument**

The sole issue on appeal is whether Appellant has properly antedated the Van Buskirk et al. Patent (Patent No. 6,001,689) to remove this Patent as a reference under 35 USC § 102 or 103 against the instant claims. Applicant has relied upon a decision by the United States Supreme Court in Pfaff v Wells Electronics, 525 US 55 (US 1998) to support the argument that 35 USC 102(b) does not require an *invention* to be reduced to practice. Applicant's arguments have been considered by the Board of Patent Appeals and Interferences in the Decision on Rehearing rendered December 31, 2003. In their decision, the Board stated that since the question before the Supreme Court in Pfaff was "whether the commercial marketing of a newly invented product may mark the beginning of the 1-year period [set forth in 35 USC 102(b)] even though the invention has not yet been reduced to practice", Pfaff has little, if any, relevance to the facts of this application, since Pfaff did not address 37 CFR 1.131. In the present case, the claims have been rejected under 35 USC 102(e) as unpatentable over Van Buskirk. Applicant has alleged that the requirements of 37 CFR 1.131 have been met to

Art Unit: 2822

effectively antedate the Van Buskirk reference. However, for the reasons already of record, Appellant has not satisfied the requirements of 37 CFR 1.131. Hence, the rejection of claims 12-19 has been maintained.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,



M. Wilczewski  
Primary Examiner Tech Center  
2800

April 4, 2005

Conferees  
Olik Chaudhuri ✓  
Amir Zarabian ✓

Jacqueline J Garner Esq  
Texas Instruments Incorporated  
P O Box 655474 M S 219  
Dallas, TX 75265